

Fig. 1

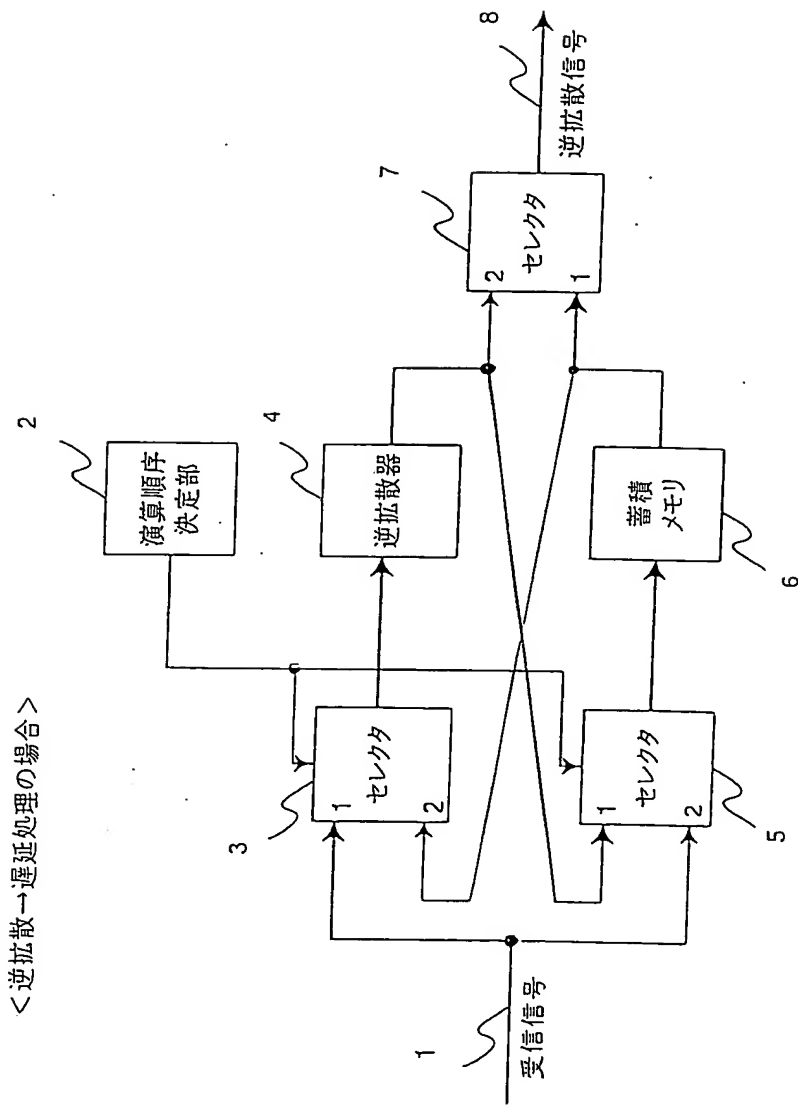


Fig. 1

<Case of reverse diffusion → delay processing>

- (1) receiving signal
- (2) calculation order determining portion
- (3) selector
- (4) reverse diffusing unit
- (5) selector
- (6) storage memory
- (7) selector
- (8) reverse diffusing signal

Fig. 2

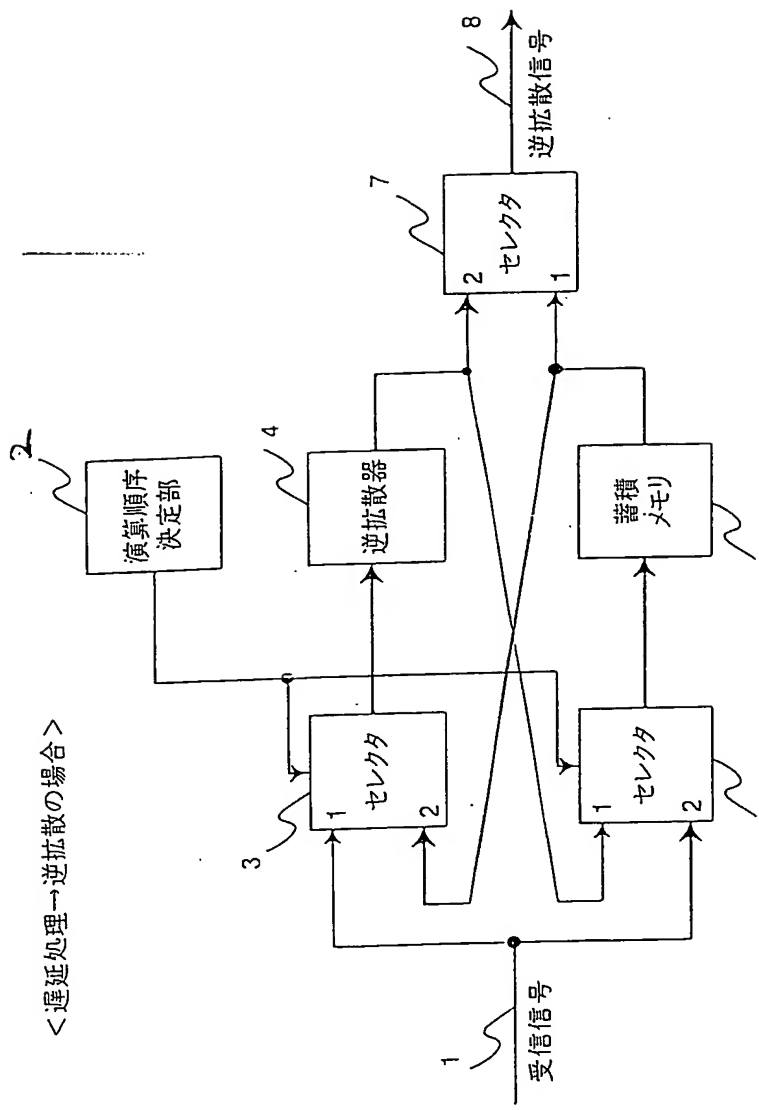
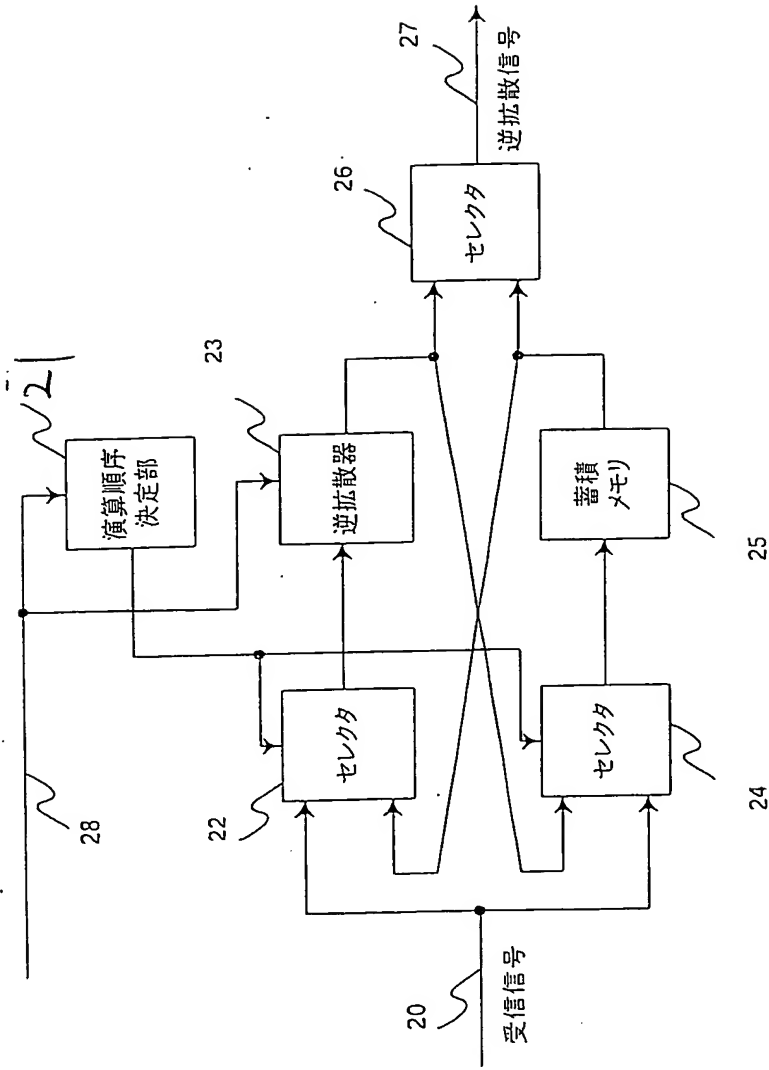


Fig. 2
<Case of delay processing → reverse diffusion>

- (1) receiving signal
- (2) calculation order determining portion
- (3) selector
- (4) reverse diffusing unit
- (5) selector
- (6) storage memory
- (7) selector
- (8) reverse diffusing signal

Fig. 3



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Fig. 3

- (20) receiving signal
- (21) calculation order determining portion
- (22) selector
- (23) reverse diffusing unit
- (24) selector
- (25) storage memory
- (26) selector
- (27) reverse diffusing signal
- (28) symbol rate information

Fig. 4

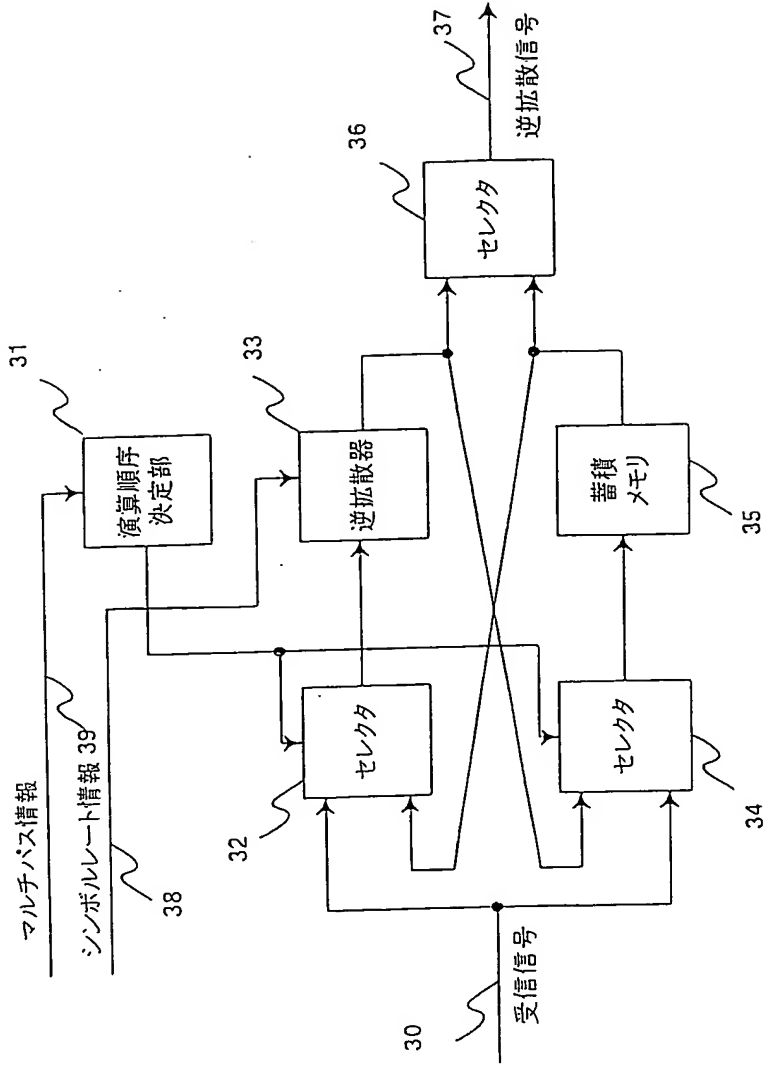


Fig. 4

- (30) receiving signal
- (31) calculation order determining portion
- (32) selector
- (33) reverse diffusing unit
- (34) selector
- (35) storage memory
- (36) selector
- (37) reverse diffusing signal
- (38) symbol rate information
- (39) multipass information

Fig. 5

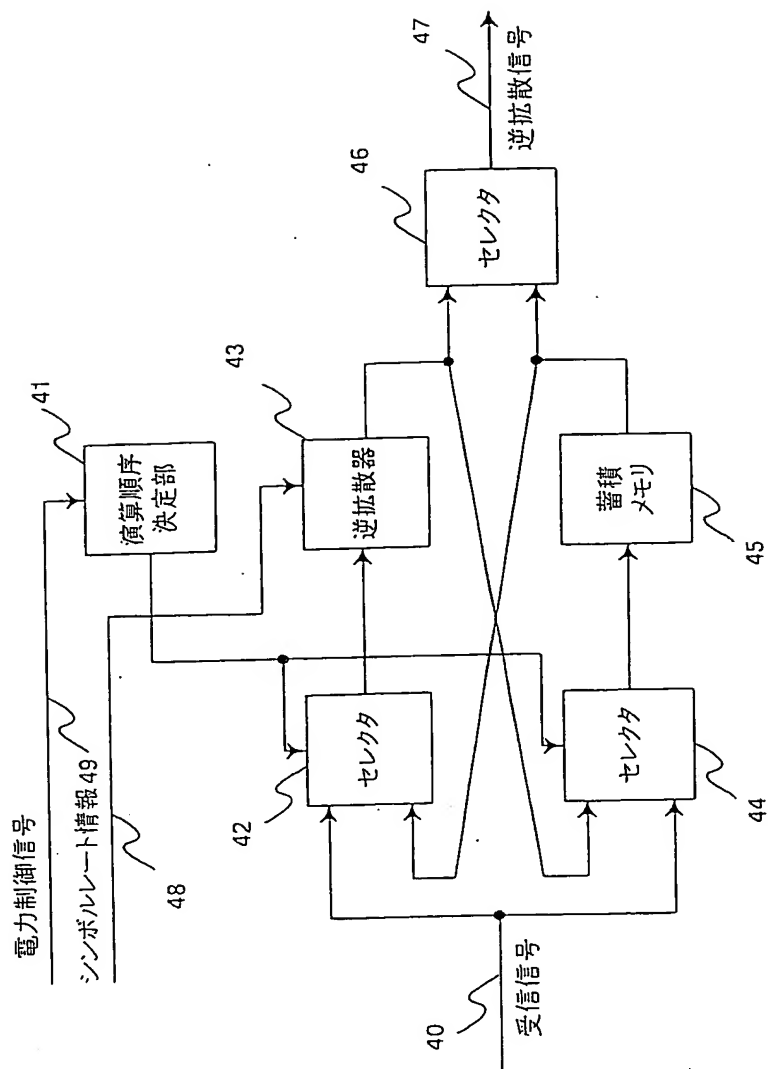


Fig. 5

- (40) receiving signal
- (41) calculation order determining portion
- (42) selector
- (43) reverse diffusing unit
- (44) selector
- (45) storage memory
- (46) selector
- (47) reverse diffusing signal
- (48) symbol rate information
- (49) power control signal

Fig. 6

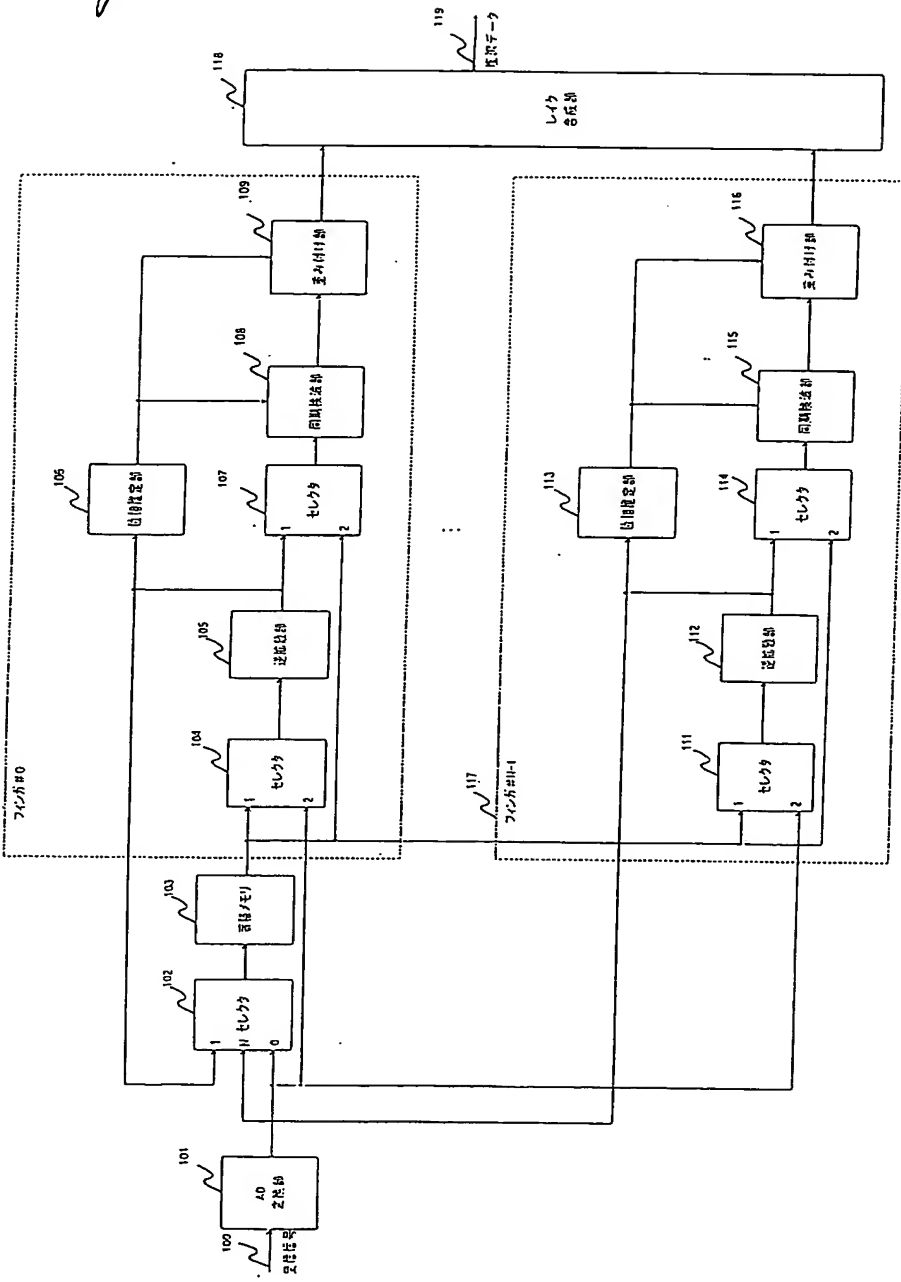
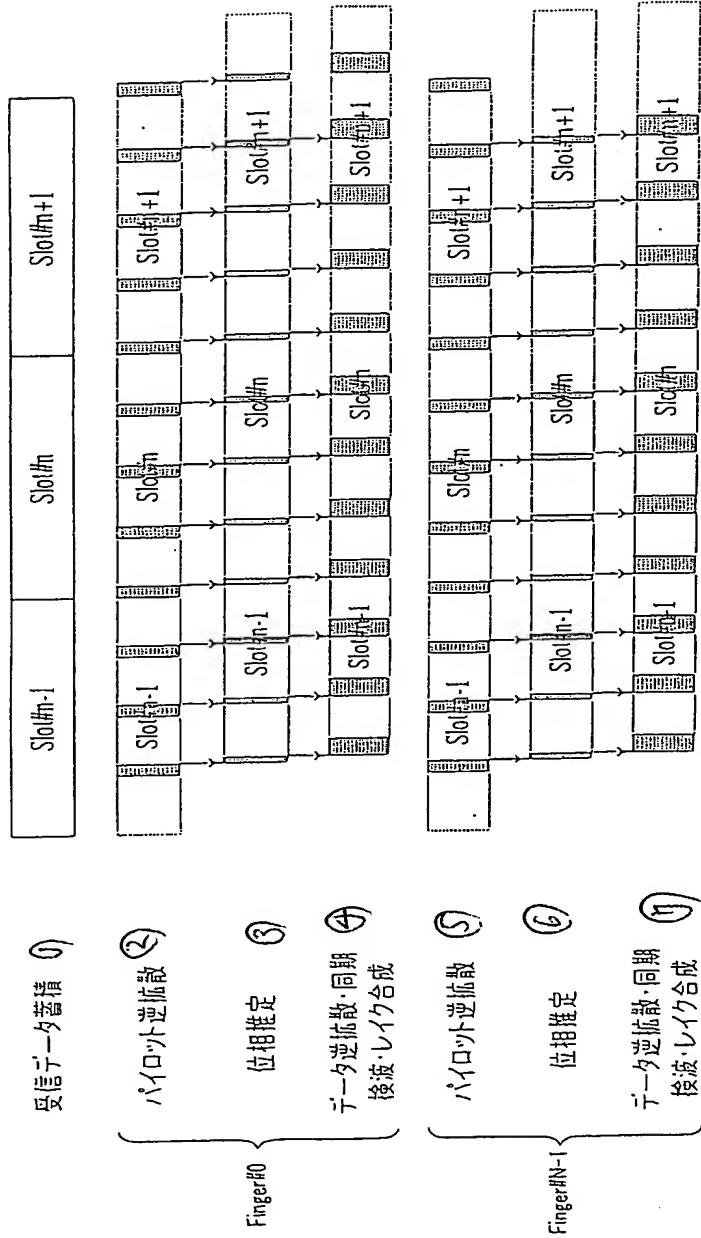


Fig. 6

- (100) receiving signal
- (101) A/D converting portion
- (102) selector
- (103) storage memory
- (104) selector
- (105) reverse diffusing portion
- (106) phase estimating portion
- (107) selector
- (108) synchronous detecting portion
- (109) weighting portion
- (110) finger
- (111) selector
- (112) reverse diffusing portion
- (113) phase estimating portion
- (114) selector
- (115) synchronous detecting portion
- (116) weighting portion
- (117) finger
- (118) rake synthesizing portion
- (119) demodulated data

Fig. 7



- ① Receive data storage
- ② Pilot reverse diffusion
- ③ Phase estimation
- ④ Data reverse diffusion □ synchronous detection □ rake synthesis
- ⑤ Pilot reverse diffusion
- ⑥ Phase estimation
- ⑦ Data reverse diffusion □ synchronous detection □ rake synthesis

Fig. 8

- (237) demodulated data

Fig. 9

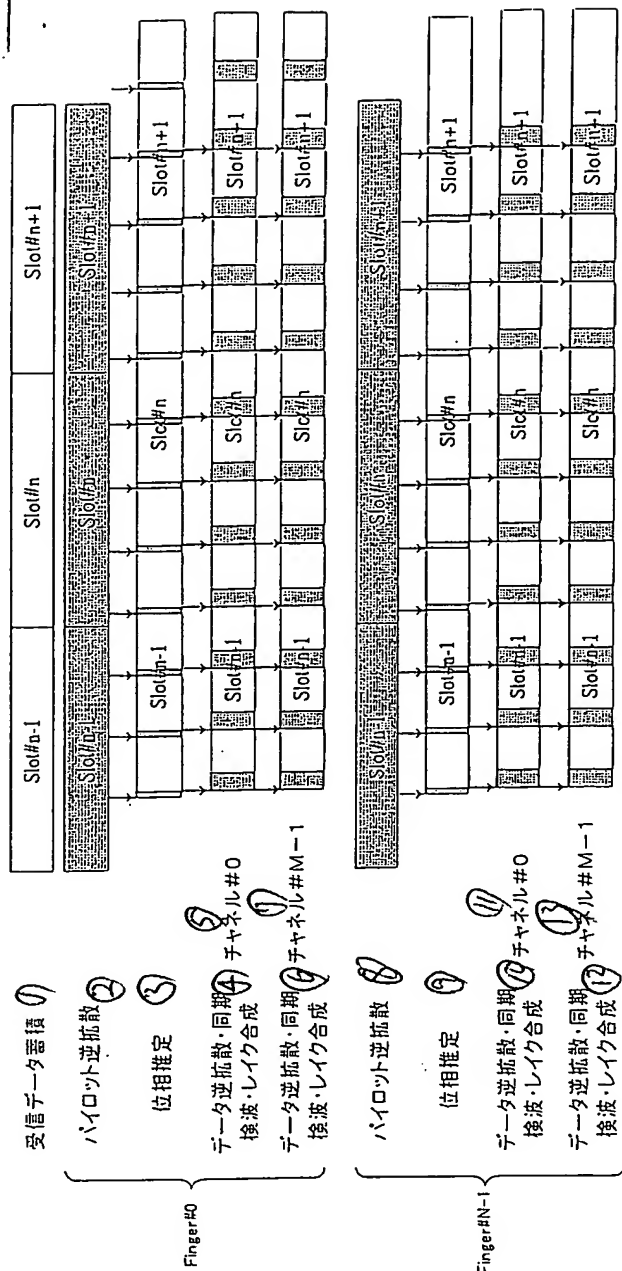


Fig. 9

- 1 Receive data storage
- 2 Pilot reverse diffusion
- 3 Phase estimation
- 4 Data reverse diffusion □ synchronous detection □ rake synthesis
- 5 Channel
- 6 Data reverse diffusion □ synchronous detection □ rake synthesis
- 7 Channel
- 8 Pilot reverse diffusion
- 9 Phase estimation
- 10 Data reverse diffusion □ synchronous detection □ rake synthesis
- 11 Channel
- 12 Data reverse diffusion □ synchronous detection □ rake synthesis
- 13 Channel

Fig. 10

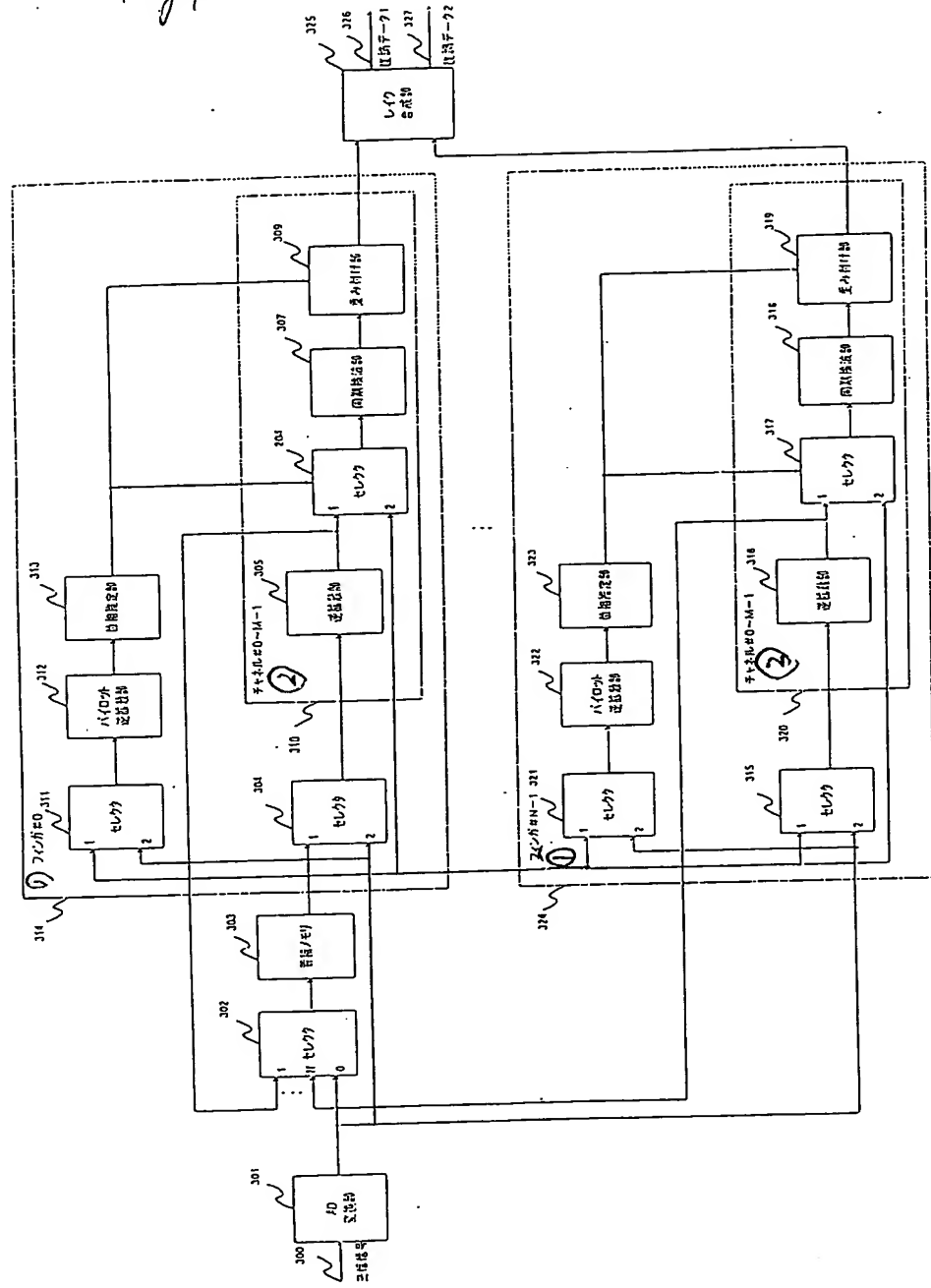


Fig. 10

- (300) receiving signal
- (301) AD converting portion
- (302) selector
- (303) storage memory
- (304) selector
- (305) reverse diffusing portion
- (306) selector
- (307) synchronous detecting portion
- (309) weighting portion
- (311) selector
- (312) pilot reverse diffusing portion
- (313) phase estimating portion
- (315) selector
- (316) reverse diffusing portion
- (317) selector
- (318) synchronous detecting portion
- (319) weighting portion
- (321) selector
- (322) pilot reverse diffusing portion
- (323) phase estimating portion
- (325) rake synthesizing portion
- (326) demodulated data
- (327) demodulated data
- Finger ①
- Channel ②

Fig. 11

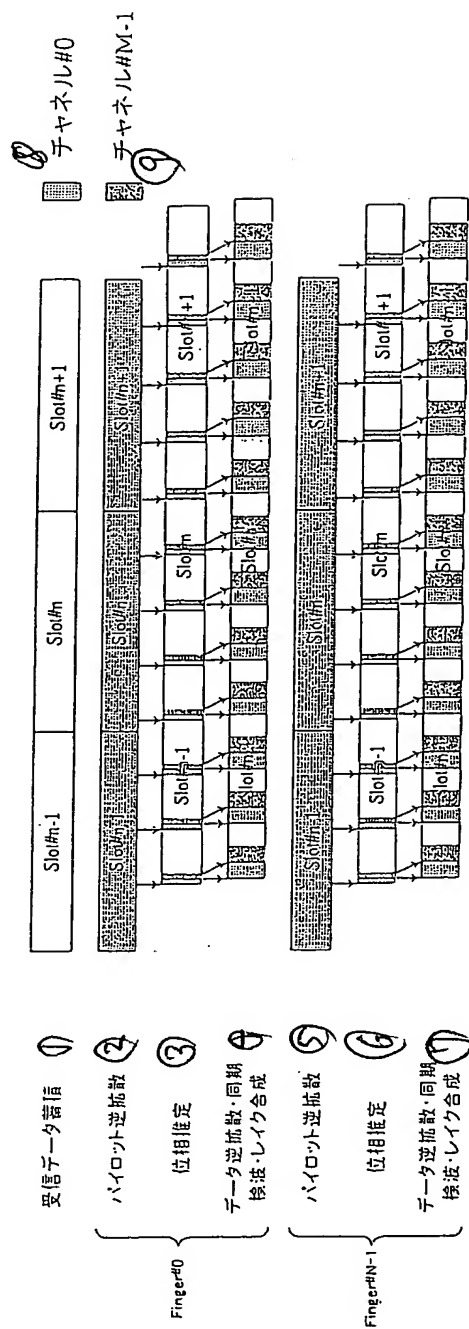


Fig. 12

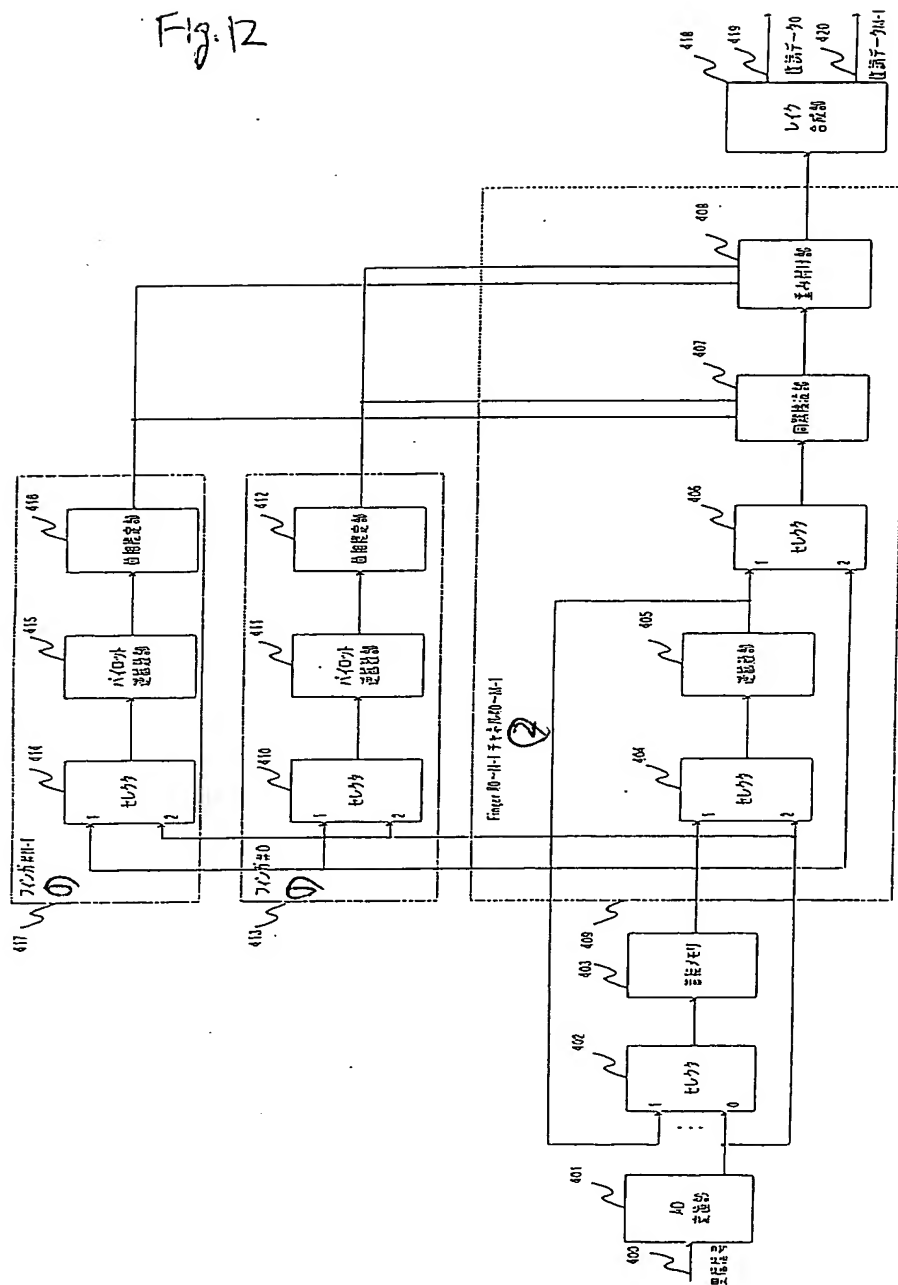


Fig. 12

- (400) receiving signal
- (401) AD converting portion
- (402) selector
- (403) storage memory
- (404) selector
- (405) reverse diffusing portion
- (406) selector
- (407) synchronous detecting portion
- (408) weighting portion
- (410) selector
- (411) pilot reverse diffusing portion
- (412) phase estimating portion
- (414) selector
- (415) pilot reverse diffusing portion
- (416) phase estimating portion
- (418) rake synthesizing portion
- (419) demodulated data
- (420) demodulated data

Finger

Channel

Fig. 13

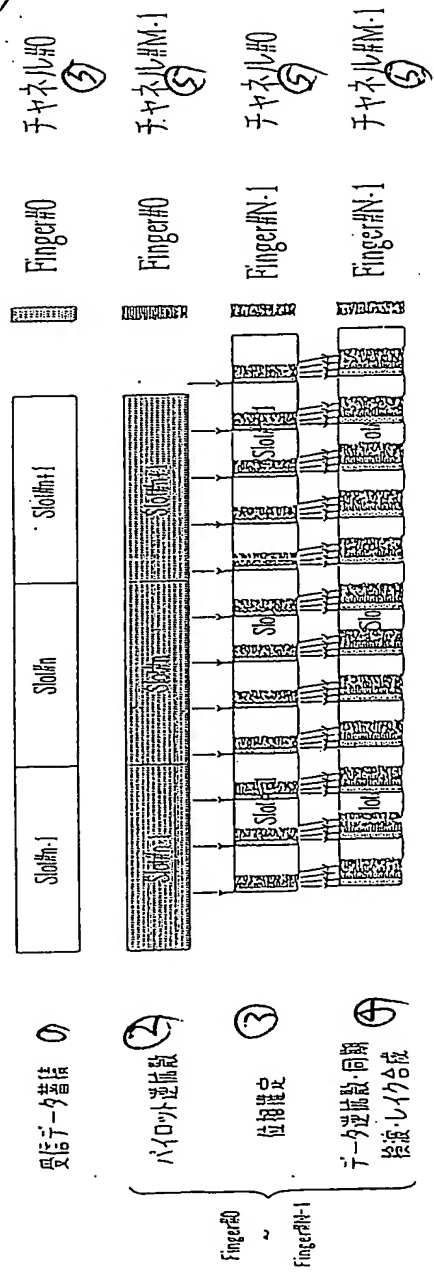


Fig. 13

- ① Receive data storage
- ② Pilot reverse diffusion
- ③ Phase estimation
- ④ Data reverse diffusion □ synchronous detection □ rake synthesis
- ⑤ Channel

Fig. 14

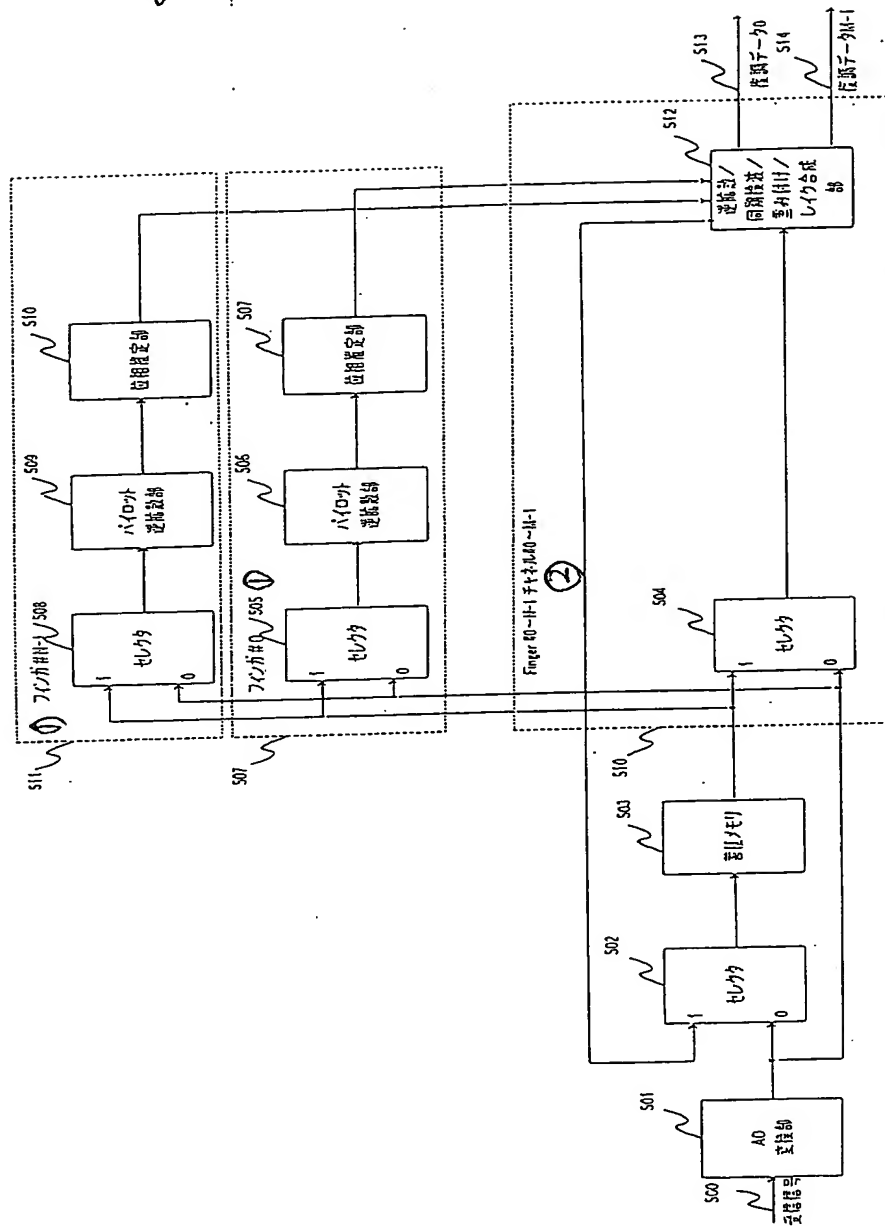


Fig. 14

- (500) receiving signal
- (501) AD converting portion
- (502) selector
- (503) storage memory
- (504) selector
- (505) selector
- (506) pilot reverse diffusing portion
- (507) phase estimating portion
- (508) selector
- (509) pilot reverse diffusing portion
- (510) phase estimating portion
- (512) reverse diffusing / synchronous detecting / weighting / rake synthesizing portion
- (513) demodulated data
- (514) demodulated data

Finger ①

Channel ②

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Fig. 15

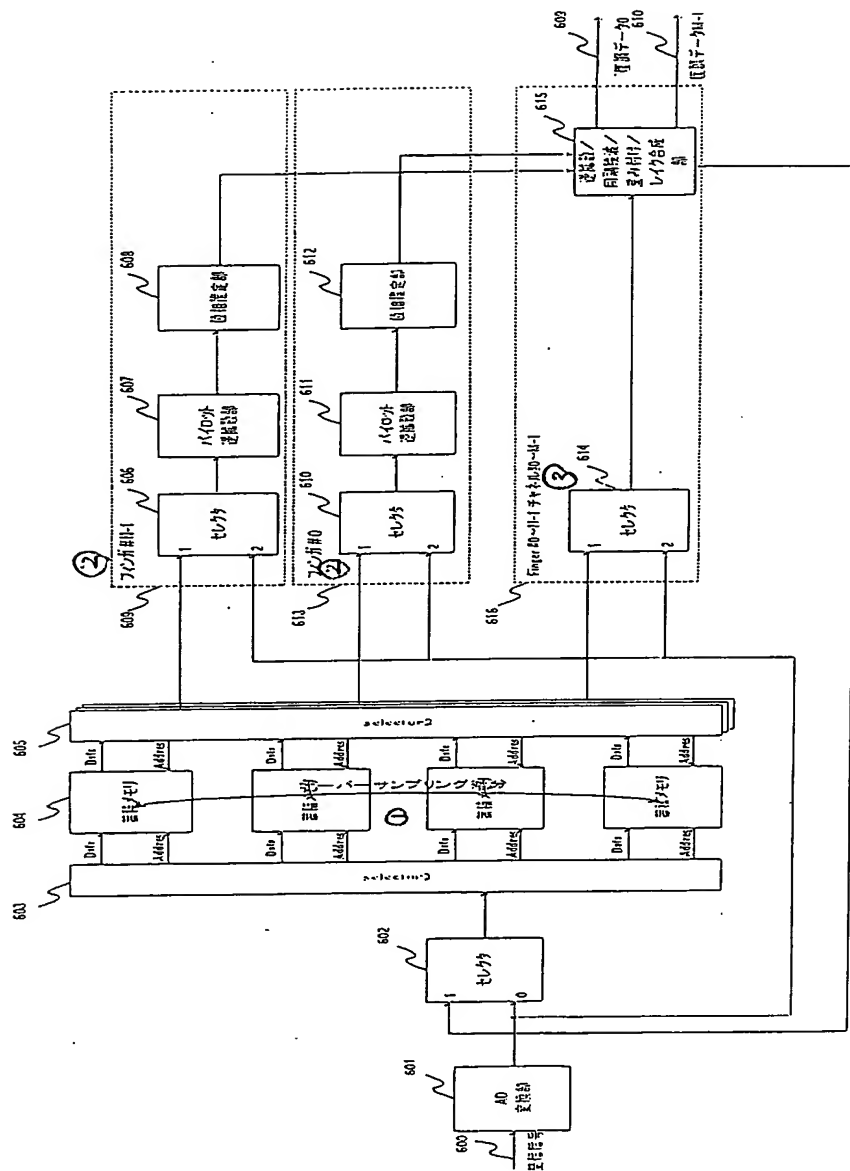


Fig. 16

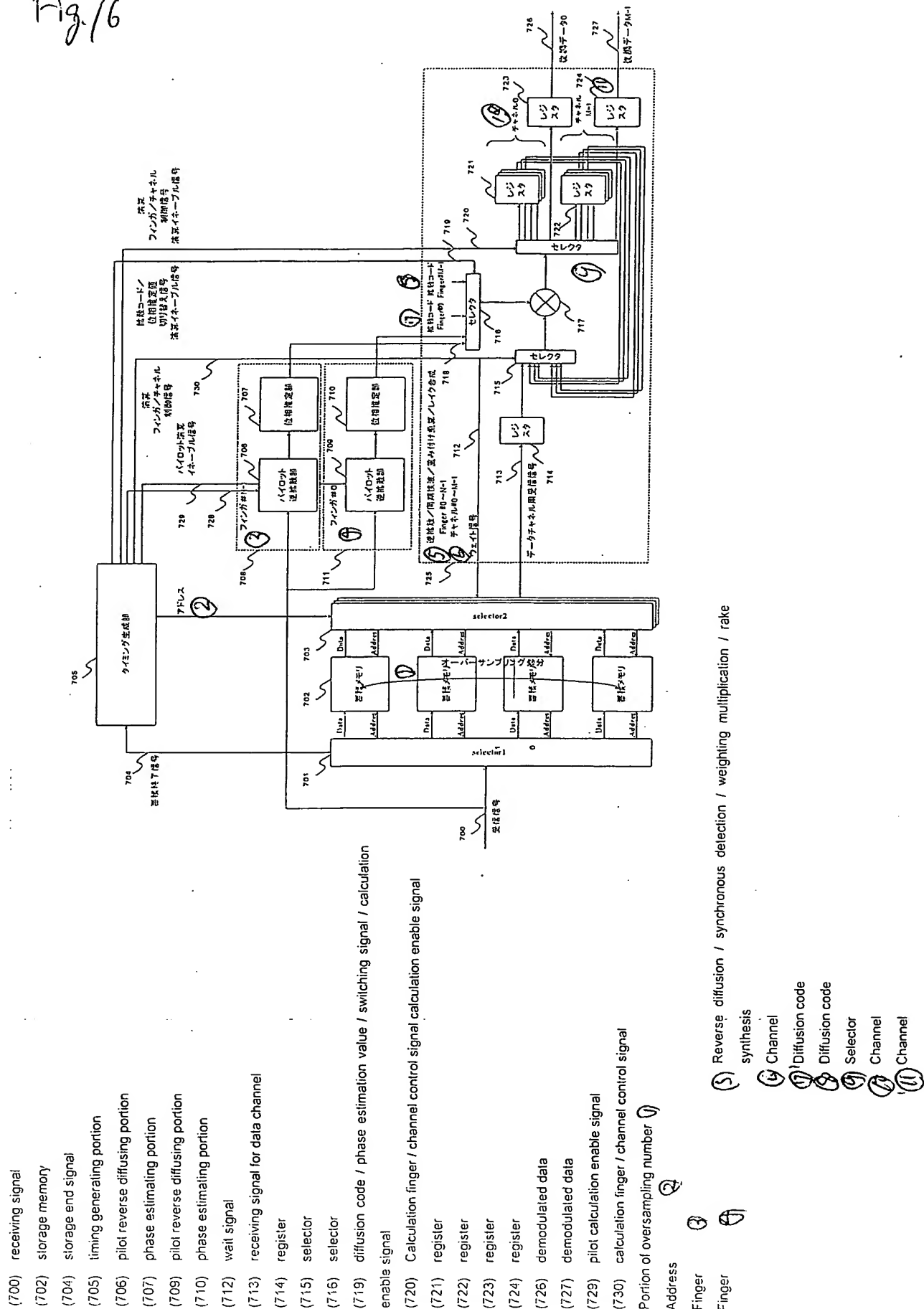
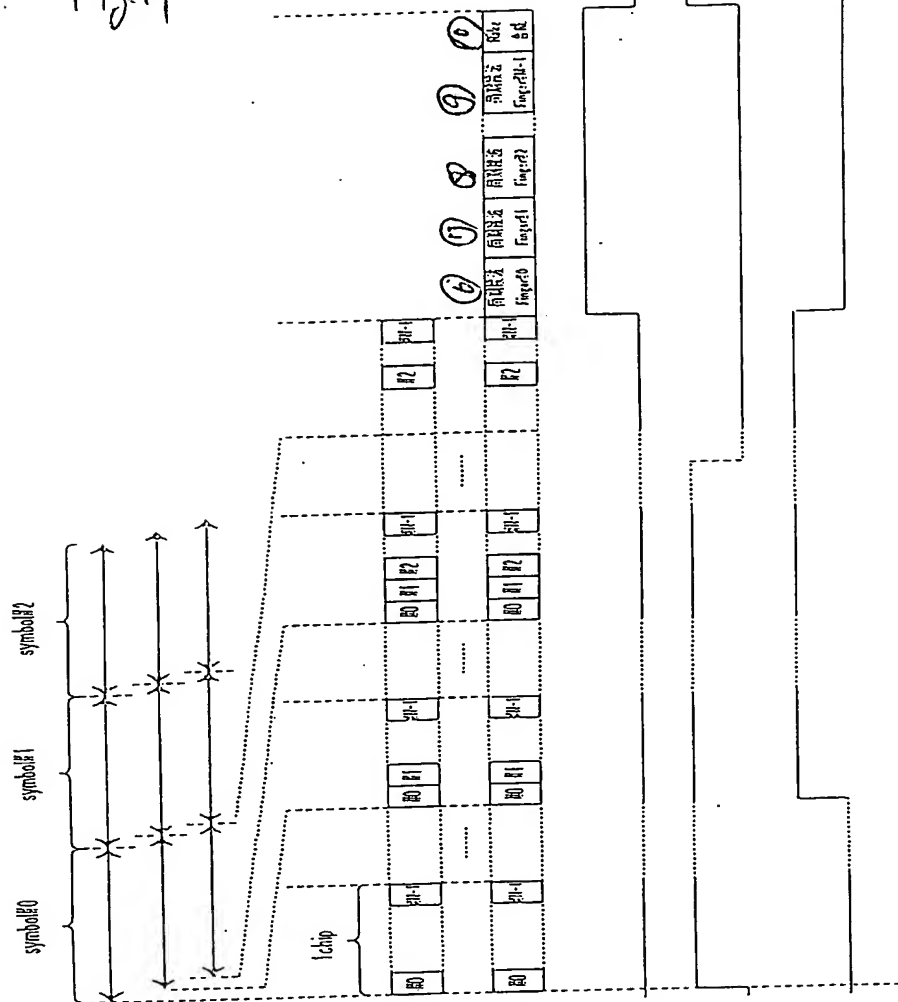


Fig. 17



- ① 下クチャヤナル用受信信号
- ② 遅延(逆分散) / 同期検波 / リーク合成
- ③ カエト信号
- ④ Finger#0遅延イネーブル信号
- ⑤ Finger#1遅延イネーブル信号

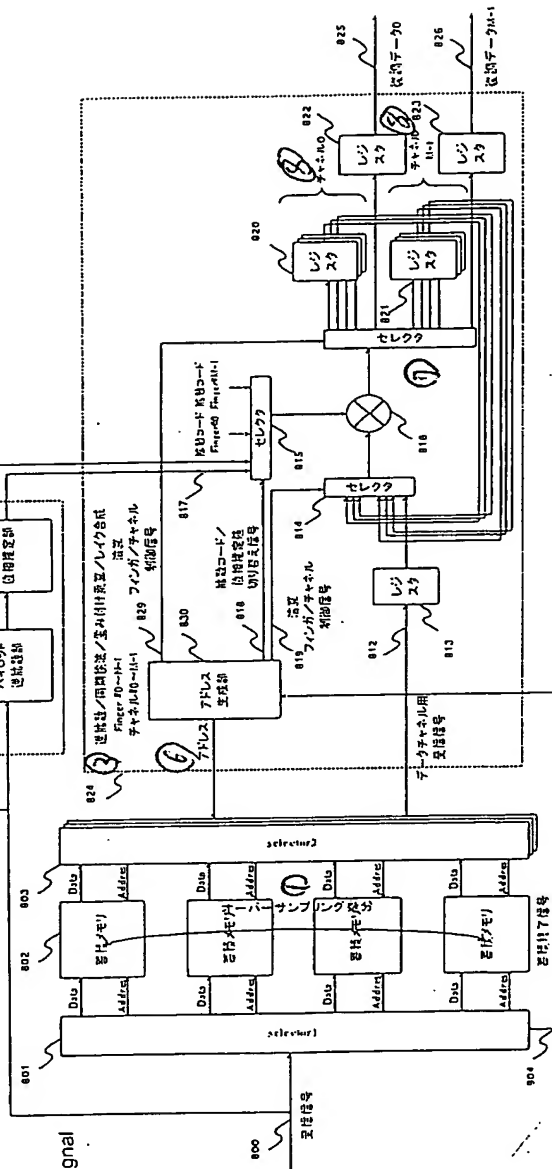
Fig. 17

- ① Receiving signal for data channel
- ② Calculation (reverse diffusion / synchronous detection / rake synthesis)
- ③ Wait signal
- ④ Calculation enable signal
- ⑤ Calculation enable signal
- ⑥ Synchronous detection
- ⑦ Synchronous detection
- ⑧ Synchronous detection
- ⑨ Synchronous detection
- ⑩ Rake synthesis

Fig. 18

Fig. 18

- (800) receiving signal
- (802) storage memory
- (804) storage end signal
- (805) limiting generating portion
- (806) pilot reverse diffusing portion
- (807) phase estimating portion
- (809) pilot reverse diffusing portion
- (810) phase estimating portion
- (812) receiving signal for data channel
- (813) register
- (814) selector
- (815) selector



- (818) diffusion code / phase estimation value switching signal
- (819) calculation finger / channel control signal
- (820) register
- (821) register
- (822) register
- (823) register
- (825) demodulated data
- (826) demodulated data
- (828) pilot calculation enable signal
- (829) calculation finger / channel control signal
- (830) address generating portion

① Portion of oversampling number
Finger

② Reverse diffusion / synchronous detection / weighting multiplication / rake
synthesis

- ③ Channel
- ④ Address
- ⑤ Diffusion code
- ⑥ Selector
- ⑦ Channel

Fig. 19

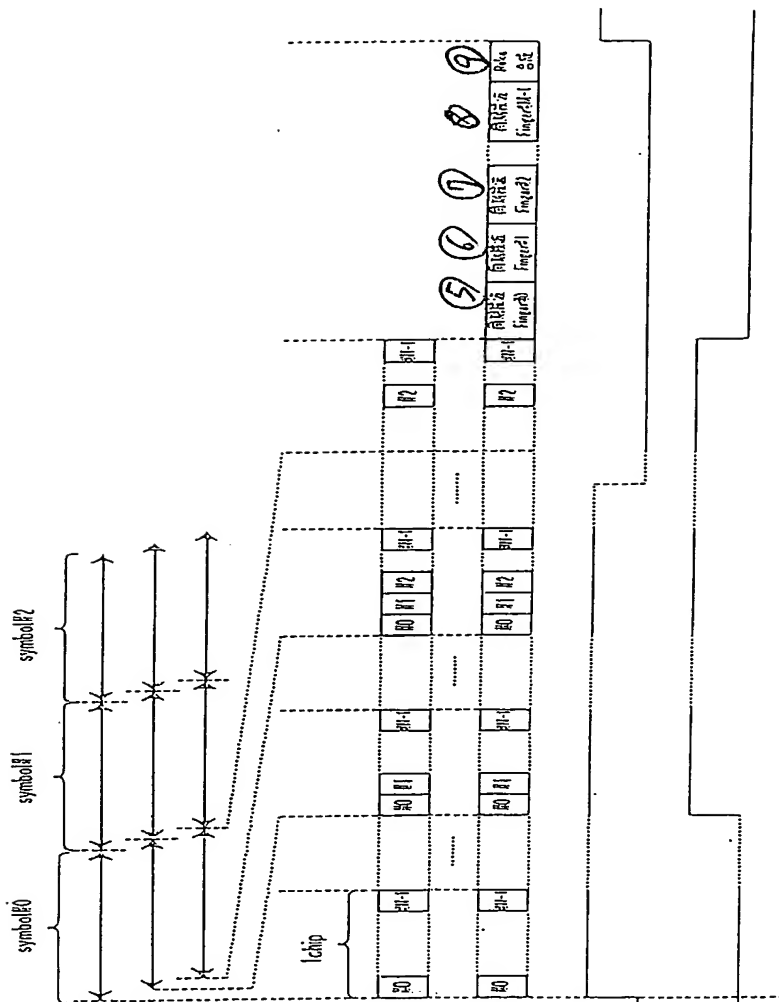


Fig. 19

① Receiving signal for data channel

② Calculation (reverse diffusion / synchronous detection / rake synthesis)

③ Calculation enable signal

④ Calculation enable signal

⑤ Synchronous detection

⑥ Synchronous detection

⑦ Synchronous detection

⑧ Synchronous detection

⑨ Rake synthesis

① データチャネル用受信信号

② 演算(逆拡散/同期検波/レイク合成)

③ Finger#0演算イネーブル番号

④ Finger#2演算イネーブル番号

Fig. 20

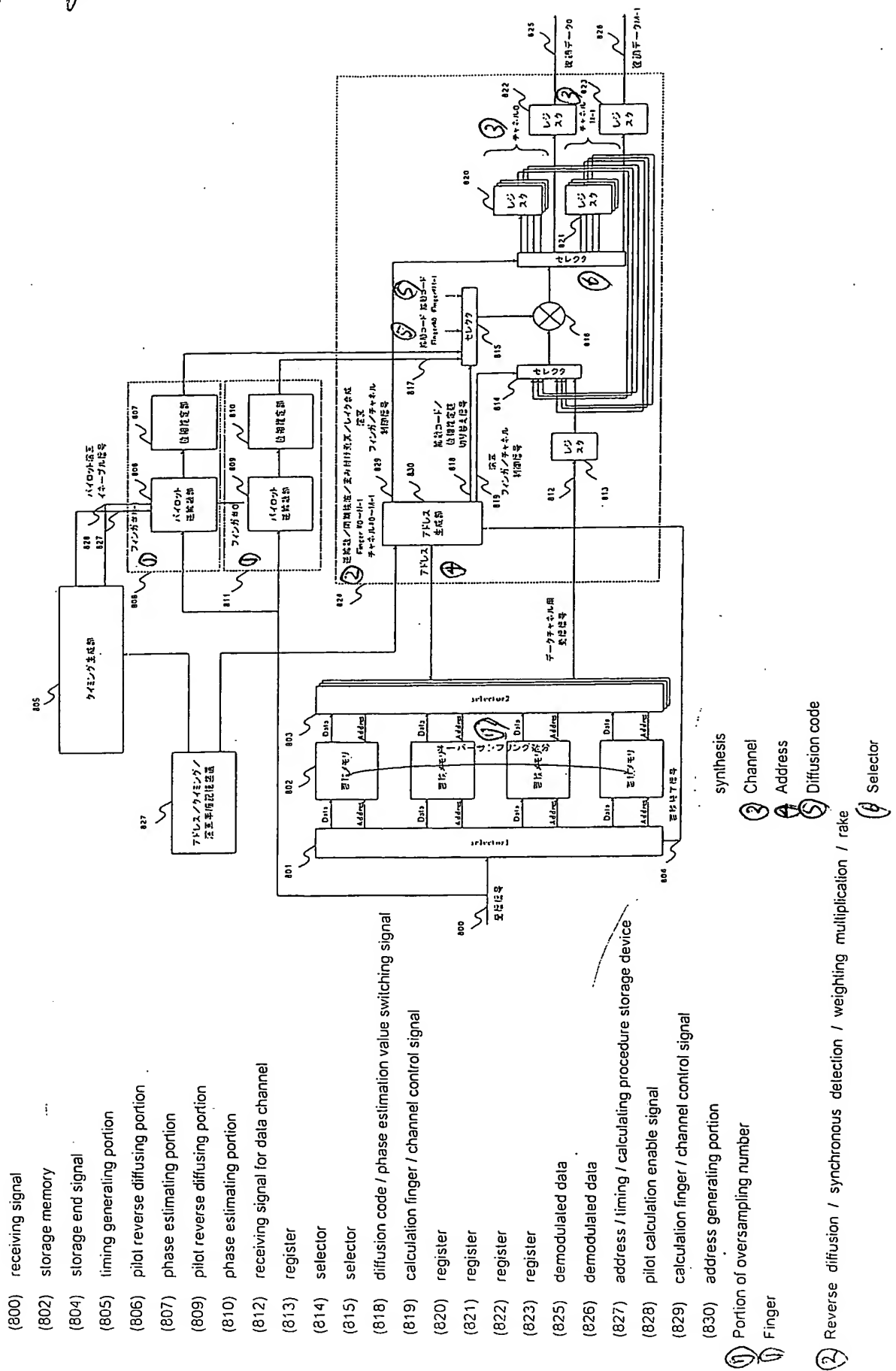
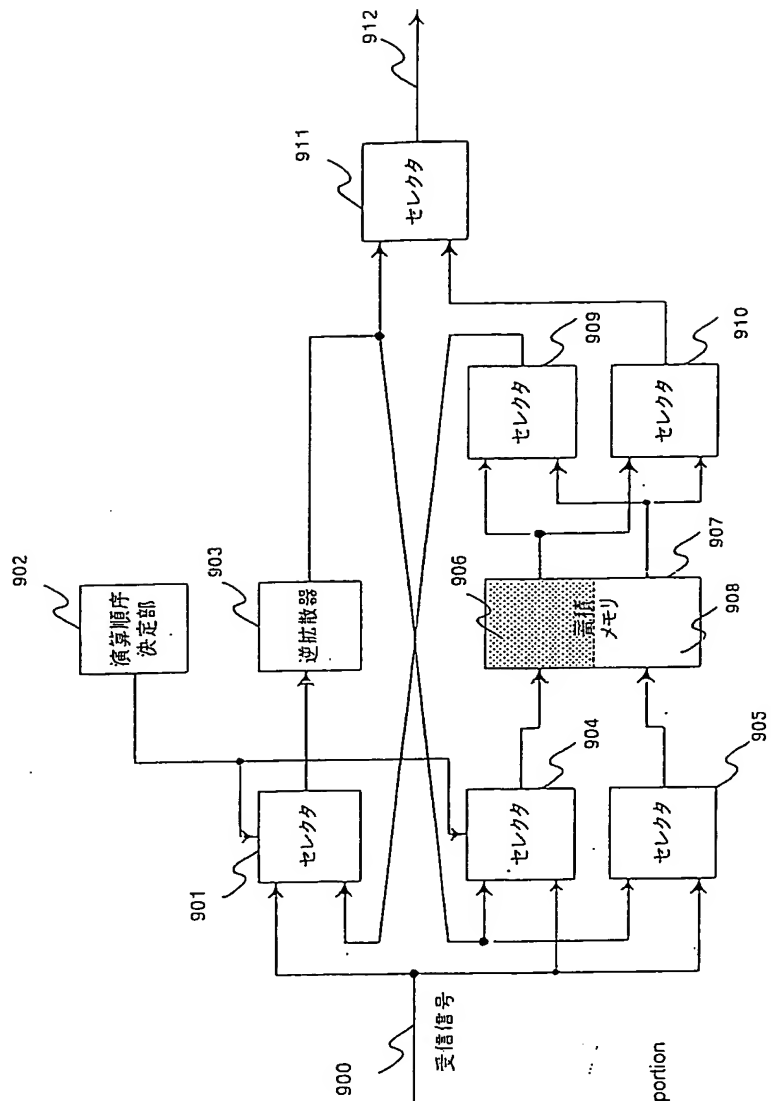


Fig. 21



- (900) receiving signal
- (901) selector
- (902) calculation order determining portion
- (903) reverse diffusing unit
- (904) selector
- (905) selector
- (907) storage memory
- (909) selector
- (910) selector
- (911) selector

Fig. 22

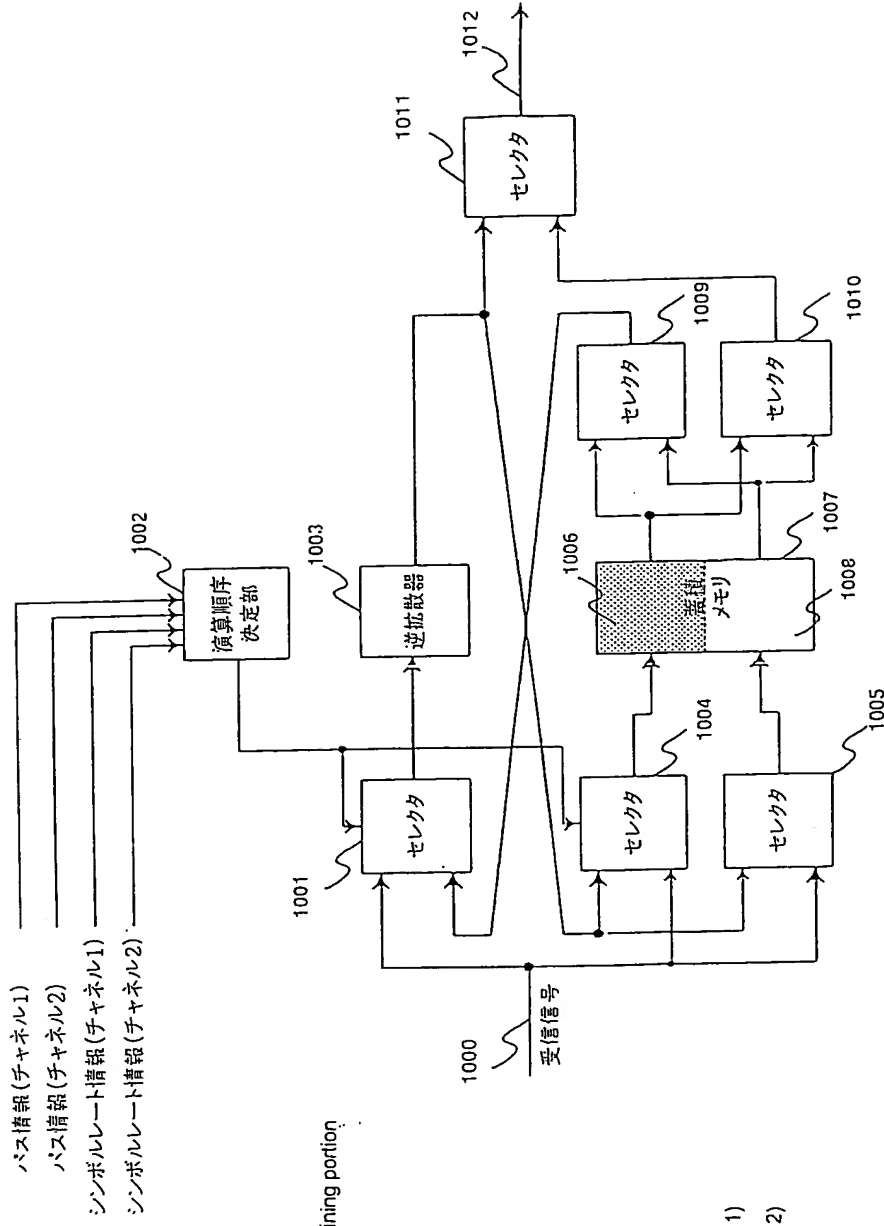


Fig. 22

- (1000) receiving signal
- (1001) selector
- (1002) calculation order determining portion
- (1003) reverse diffusing unit
- (1004) selector
- (1005) selector
- (1006) storage memory
- (1007) selector
- (1008) selector
- (1009) selector
- (1010) selector
- (1011) selector
- Pass information (channel 1)
- Pass information (channel 2)
- Symbol rate information (channel 1)
- Symbol rate information (channel 2)

Fig.23

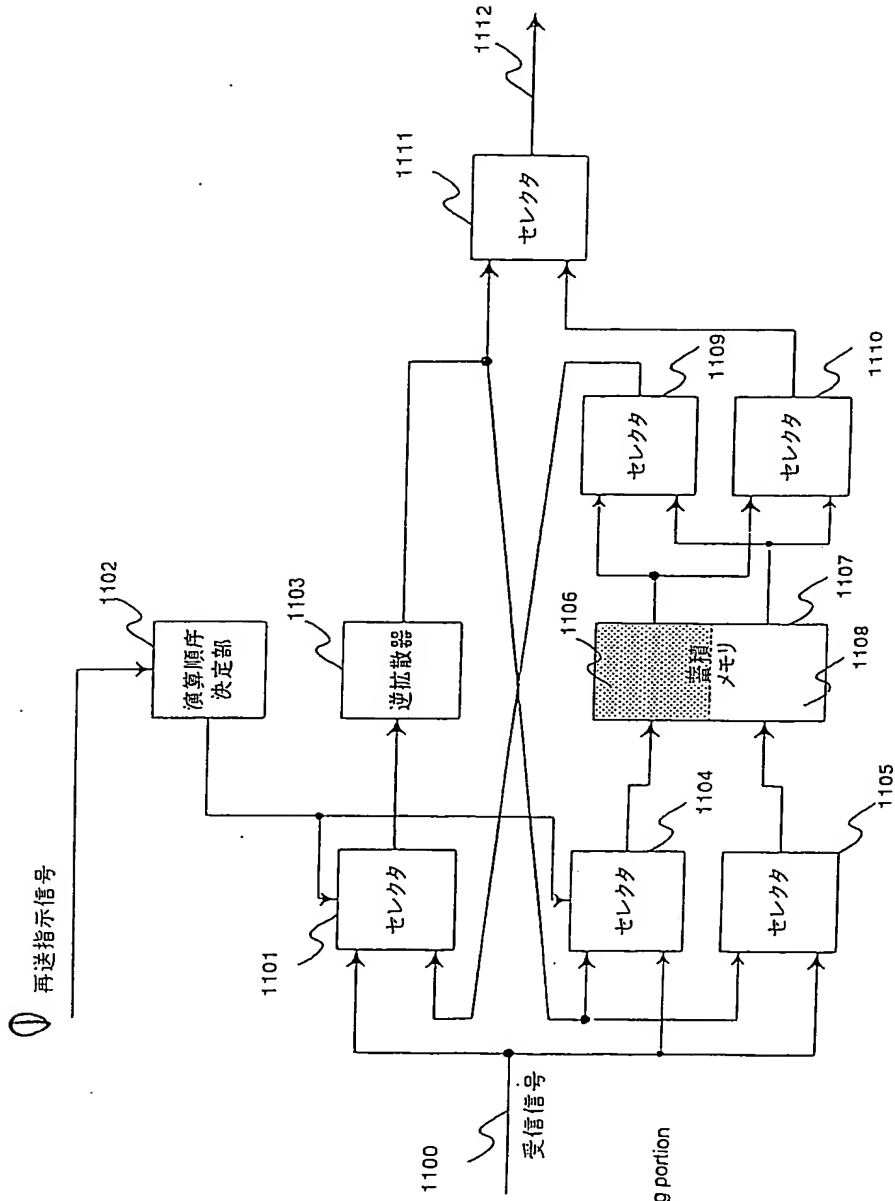
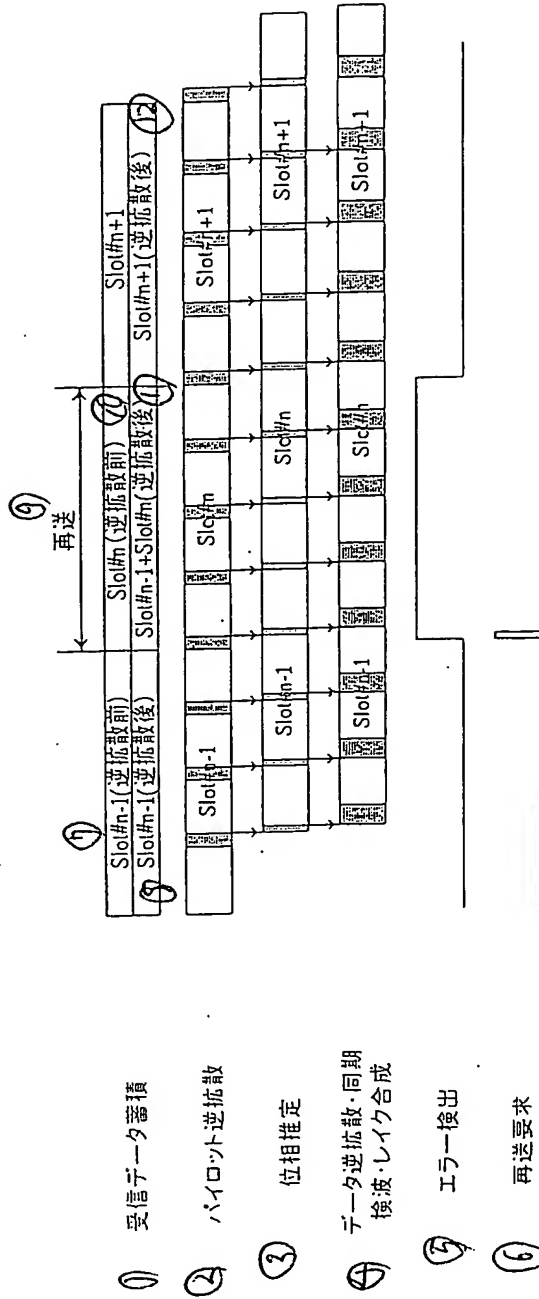


Fig. 23

- (1100) receiving signal
- (1101) selector
- (1102) calculation order determining portion
- (1103) reverse diffusing unit
- (1104) selector
- (1105) selector
- (1107) storage memory
- (1109) selector
- (1110) selector
- (1111) selector

Retransmission indicating signal ①

F-18.24

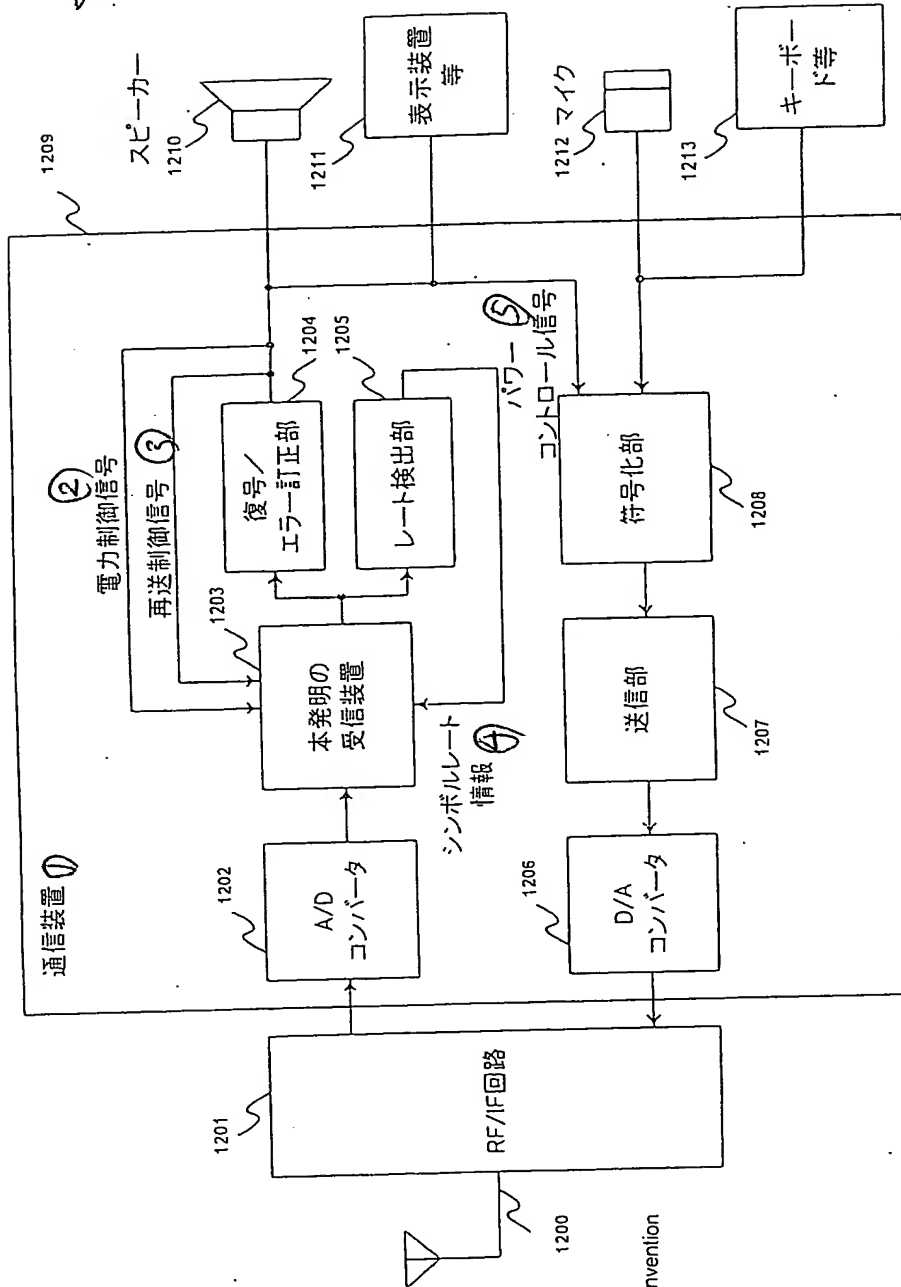


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Fig. 24

- ① Receive data storage
- ② Pilot reverse diffusion
- ③ Phase estimation
- ④ Data reverse diffusion & synchronous detection & rake synthesis
- ⑤ Error detection
- ⑥ Retransmission request
- ⑦ Before reverse diffusion
- ⑧ After reverse diffusion
- ⑨ Retransmission
- ⑩ Before reverse diffusion
- ⑪ After reverse diffusion
- ⑫ After reverse diffusion

Fig. 25



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Fig. 25

(1201) RF/IF circuit

(1202) A/D converter

(1203) receiving device according to the invention

(1204) decoding / error correcting portion

(1205) rate detecting portion

(1206) D/A converter

(1207) transmitting portion

(1208) coding portion

(1210) speaker

(1211) display device

(1212) microphone

(1213) keyboard

① Communicating device

② Power control signal

③ Retransmission control signal

④ Symbol rate information

⑤ Power control signal

Fig. 26

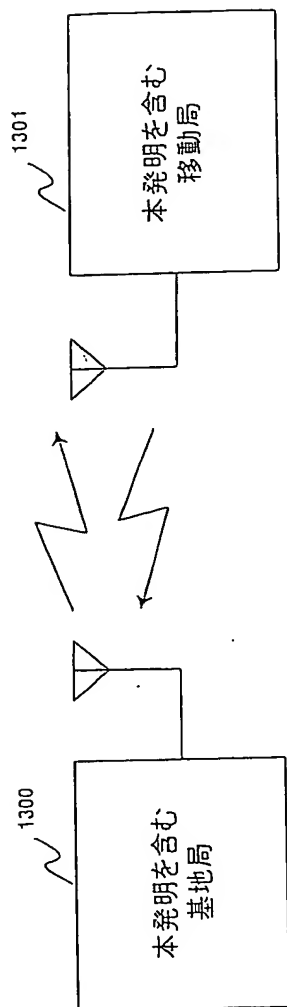


Fig. 26

(1300) base station including the invention

(1301) mobile station including the invention

F18.27

<Conditions>

W-CDMA method

Number of channels 15

Number of receive data bits 6

Number of finger passes 12

Storage time 1 slot

Diffusion rate 4

Total number of bits of memory

Case of symbol buffer after reverse diffusion

Number of input bits

Amplification increase rate by reverse diffusion

Number of finger passes

Number of symbols in slot

Number of channels

14000 bits

Case of receive data buffer

Number of input bits

Number of samples in slot

122880 bits

<条件>

・W-CDMA方式

・チャネル数15

・受信データビット数6

・フィンガパス数12

・蓄積時間1スロット

・拡散率4

	逆拡散後シンボルバツファの場合	受信データバツファの場合
メモリ総ビット数	6 (入力ビット数) $\times 5 \text{ (逆拡散による振幅増加倍率)}$ $\times 12 \text{ (フィンガパス数)}$ $\times (2560 / 16) \text{ (スロット内シンボル数)}$ $\times 15 \text{ (チャネル数)}$ $\times 2 \text{ (IQ)}$ $= 144000 \text{ ビット}$	6 (入力ビット数) $\times (2560 \times 4) \text{ (スロット内サンプル数)}$ $\times 2 \text{ (IQ)}$ $= 122880 \text{ ビット}$

Fig. 28

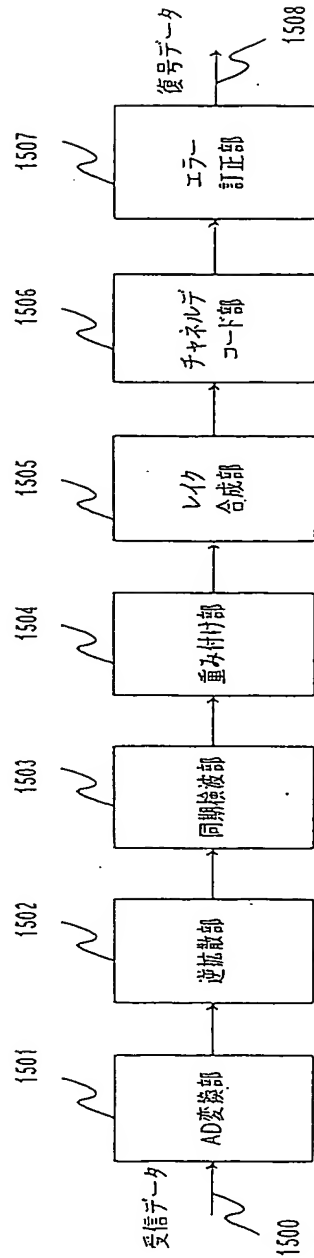
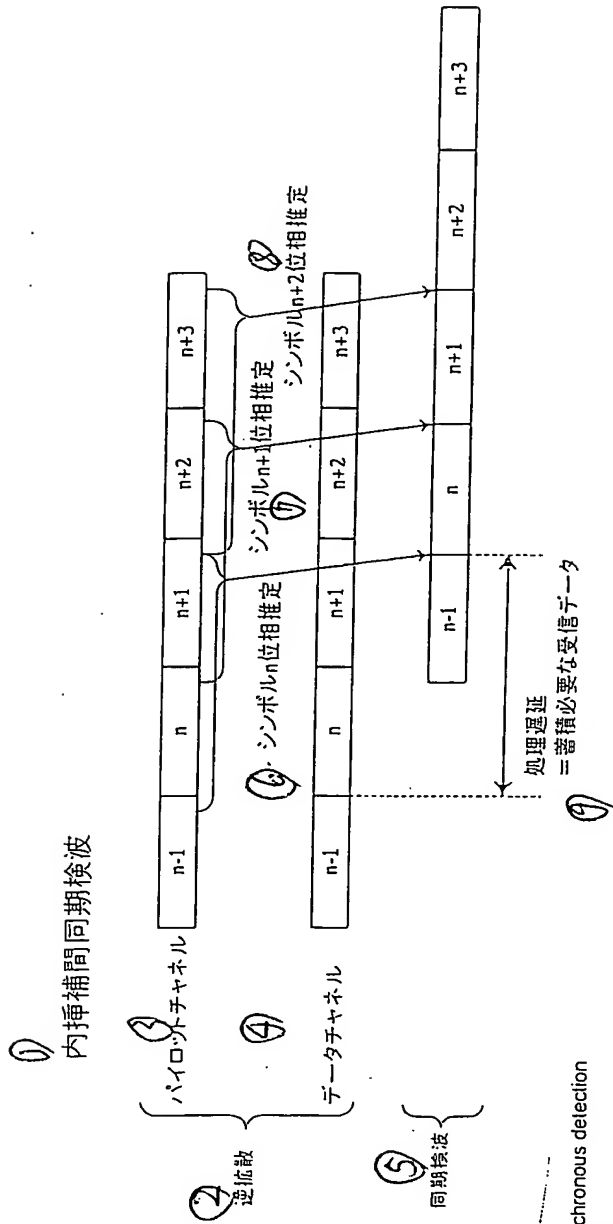


Fig. 28

- (1500) Receive data
- (1501) AD converting portion
- (1502) reverse diffusing portion
- (1503) synchronous detecting portion
- (1504) weighing portion
- (1505) rake synthesizing portion
- (1506) channel decoding portion
- (1507) error correcting portion
- (1508) decode data

Fig. 29



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Fig. 29

① Interpolating synchronous detection

② Reverse diffusion

③ Pilot channel

④ Data channel

⑤ Synchronous detection

⑥ Symbol n phase estimation

⑦ Symbol $n+1$ phase estimation

⑧ Symbol $n+2$ phase estimation

⑨ Processing delay = receive data required to be stored

Fig. 30

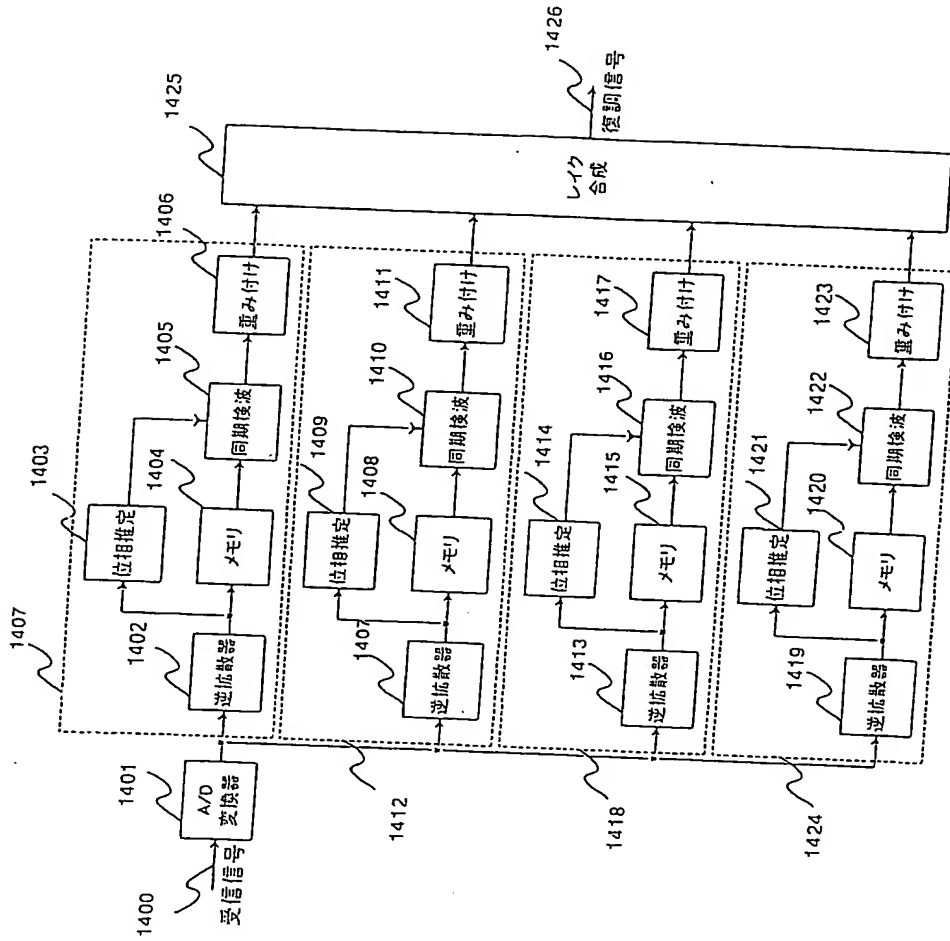
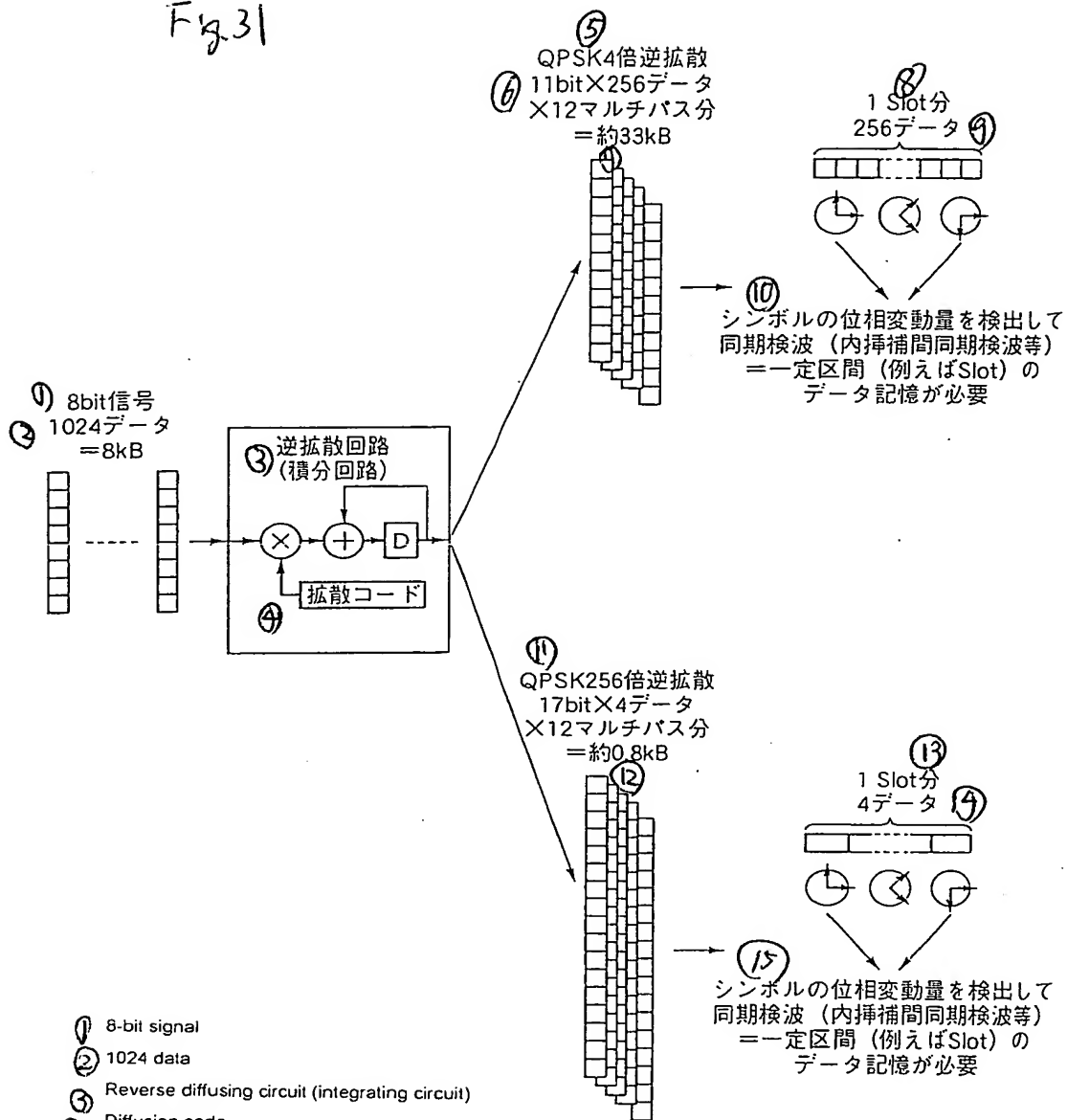


Fig. 30

- (1400) receiving signal
- (1401) A/D converter
- (1402) reverse diffusing unit
- (1403) phase estimation
- (1404) memory
- (1405) synchronous detection
- (1406) weighing
- (1407) reverse diffusing unit
- (1408) memory
- (1409) phase estimation
- (1410) synchronous detection
- (1411) weighing
- (1413) reverse diffusing unit
- (1414) phase estimation
- (1415) memory
- (1416) synchronous detection
- (1417) weighing
- (1419) reverse diffusing unit
- (1420) memory
- (1421) phase estimation
- (1422) synchronous detection
- (1423) weighing
- (1425) rake synthesis
- (1426) demodulating signal

Fig. 31



- ① 8-bit signal
- ② 1024 data
- ③ Reverse diffusing circuit (integrating circuit)
- ④ Diffusion code
- ⑤ 4-time reverse diffusion
- ⑥ Portion of 11 bit X 256 data X 12 multipasses
- ⑦ Approximately
- ⑧ 1 Slot portion
- ⑨ Data
- ⑩ Detect amount of phase fluctuation of symbol and carry out synchronous detection (interpolating synchronous detection) = require storage of data for constant section (for example, Slot)
- ⑪ Portion of QPSK256-time reverse diffusion 17 bit X 4 data X 12 multipass
- ⑫ Approximately
- ⑬ 1 Slot portion
- ⑭ Data
- ⑮ Detect amount of phase fluctuation of symbol and carry out synchronous detection (interpolating synchronous detection) = require storage of data for constant section (for example, Slot)